REMARKS

Claims 1-38 are pending in this application. Claims 1, 11-17, 24 and 26-38 have been amended in several particulars for purposes of clarity and brevity that are unrelated to patentability and prior art rejections in accordance with current Office policy, to further and alternatively define Applicants' disclosed invention and to assist the Examiner to expedite compact prosecution of the instant application.

The Examiner has requested submission of a clean copy of the marked-up specification filed on November 27, 2001 because the handwritten changes were too small and difficult to read, and a statement that the Substitute Specification contains no new matter. Pursuant to the Examiner's request, a better version of the marked-up copy is enclosed as Exhibit "A". However, the original specification will **not** be marked up again or unnecessarily duplicated. Rather, Applicants hereby certify that the Substitute Specification as filed on November 27, 2001 is accurate and contains no new matter. Such a certification is sufficient under the MPEP and, as a result, entry of such a Substitute Specification is respectfully requested.

The drawings have been objected to as failing to comply with 37 C.F.R. §1.84(a)(4) because reference characters "5" and "10" are both used to designate pixel. In actually, reference "10" is used to designate a pixel, and reference "5" is used to designate a data line, as shown, for example, in FIG. 5 and FIG. 6. Accordingly, FIG. 1 has been amended to reflect the correction designation, as shown in the attached Exhibit "B" and Exhibit "C".

Claims 34 and 38 have been objected to because these dependent claims cannot be dependent from Claim X and Claim Y. In response thereto, claims 34 and 38 have been amended to overcome the objection.

Claim 34 has been rejected under 35 U.S.C. §112, 1st paragraph, as failing to comply with the enable requirement. Specifically, the Examiner asserts that it is unclear as to how the rewriting the entire display after a portion has already been carried out. In response thereto, claim 34 has been amended to overcome the rejection.

Claims 1, 9, 11, 14-17, 21-23, 24, 26, 27, 29-31 and 36-38 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al., U.S. Patent No. 5,627,557 in view of Tanaka et al., U.S. Patent No. 5,594,464 for reasons stated on pages 4-9 of the Office Action (Paper No. 3). Specifically, in support of Applicants' base claim 1, the Examiner asserts that Yamaguchi '557 discloses all features except for "a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, the Examiner cites column 19, lines 38-61 of Tanaka '464 for allegedly disclosing "a liquid crystal display device having a reset pulse applied in order to clear the previous display state before applying the signal for controlling the next display state" in order to support an assertion that "it would have been obvious ... to allow the reset pulse as taught by Tanaka" to arrive at Applicants' base claim 1.

However, the Examiner's assessment of what Yamaguchi '557 discloses is incorrect. Likewise, the Examiner's citation of Tanaka '464, as a secondary reference, is also misplaced. As a result, this rejection is respectfully traversed for the following reasons.

Base claim 1 defines an image display apparatus comprising:

> a plurality of display pixels arranged in a matrix to provide image display, each of said display pixels having a pixel electrode and a pixel switch connected to said pixel electrode in series;
> a plurality of memory elements for storing display data;

image signal generating means for outputting a given image signal based on said display data;

a group of signal lines for connecting said image signal generating means to a group of pixel switches; and

display image selection means for writing said image signal in a given display pixel through said group of signal lines and a group of pixel switches,

wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET.

As defined in Applicants' base claim 1, each basic unit of the memory element comprises the memory switch, the memory capacitor connected to the memory switch, the amplifier field-effect transistor (FET) and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in the memory capacitor using the amplifier FET. Such an amplifier FET is used as the low electric power consumption of the sense amplifier during the data reading-out from the memory cell, as described on page 3, lines 11-21, page 9, lines 5-18, and FIG. 2 of Applicants' specification. In addition, the "refresh" operation as described, for example, on page 17, lines 7-10 of Applicants' specification, refers to the rewriting of previous data stored in the memory cell.

In contrast to Applicant's base claim 1, Yamaguchi '557 discloses a display apparatus, as shown in FIG. 14, in which a pixel is provided with a holding capacitance as a capacitance element and a pixel capacitance as a display element, as shown in FIG. 1. The purpose of Yamaguchi '557 is to remove the effect of a large leak current in the pixel capacitance, as described on column 1, lines 31-35, and column 2, lines 24-31. In order to achieve this purpose, Yamaguchi '557 utilizes

a transistor provided in a memory cell as a buffer to drive the pixel capacitance having the large leak current.

According to Yamaguchi '557, on the cited column 16, lines 46-55 and FIG. 16, the "refresh" is used in the context of "elimination (cancellation, clear, deletion) of the previous data, which has already read out from the image element capacitor. Such a refresh operation is **not**, and can**not** be interpreted to read on Applicants' claimed "refreshing operation means [part of the memory element] for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET" as expressly defined in Applicants' base claim 1.

Tanaka '464, as a secondary reference, does **not** remedy the noted deficiencies of Yamaguchi '557 in order to arrive at Applicants' base claim 1. This is because Tanaka '464 only discloses a high-speed multiplex driven liquid crystal display device, as shown in FIG. 1, in which a bistable nematic liquid crystal medium is used while maintaining high contrast, fast switching capability and a wide viewing angle.

Nevertheless, the Examiner cites column 19, lines 38-61 of Tanaka '464 for allegedly disclosing "a liquid crystal display device having a reset pulse applied in order to clear the previous display state before applying the signal for controlling the next display state" in order to support an assertion that "it would have been obvious ... to allow the reset pulse as taught by Tanaka" to arrive at Applicants' base claim 1.

This citation is misplaced, however. The cited column 19, lines 38-61 of Tanaka '464 does refer to the application of a reset pulse to clear the previous display state before applying the signals for controlling the next display state. However, such a reset pulse is used to indicate (means) the elimination (cancel,

clear) of the previous data. This is contrary to Applicants' claimed "refresh operation" in which such a "refresh operation" indicates (means, shows) the "rewriting of the previous data" stored in the memory cell.

As a result, there is **no** disclosure anywhere from the Examiner's proposed combination of Yamaguchi '557 and Tanaka '464 of Applicants' claimed "memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET" as expressly defined in Applicants' base claim 1.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, the Examiner must show that the prior art reference (or references when combined) must teach or suggest all the claim limitations, and that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings, provided with a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not** based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143. In other words, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USQP 494, 496 (CCPA 1970). Moreover, "obviousness cannot be established by combining the

teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." ACS Hospital System, Inc v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The Examiner must point to something in the prior art that suggests in some way a modification of a particular reference or a combination of references in order to arrive at Applicants' claimed invention. Absent such a showing, the Examiner has improperly used Applicants' disclosure as an instruction book on how to reconstruct to the prior art to arrive at Applicants' claimed invention.

Furthermore, any deficiencies in the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". See In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002).

In the present situation, both Yamaguchi '557 and Tanaka '464 fail to disclose and suggest key features of Applicants' base claim 1. Therefore, Applicants respectfully request that the rejection of Applicants' base claim 1 and its dependent claims be withdrawn.

With respect to Applicants' base claims 29, 31, 36, 37 and 38, Applicants respectfully traverse the rejection for the same reasons presented against the rejection of Applicants' base claim 1.

Dependent claims 2-8, 10, 18-20 and 24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al., U.S. Patent No. 5,627,557 in view of Tanaka et al., U.S. Patent No. 5,594,464 as applied to claim 1 above, and further in view of Parks, U.S. Patent No. 5,471,225 for reasons stated on pages 9-11 of the Office Action (Paper No. 3). Since the correctness of this rejection is predicated upon the correctness of the rejection of Applicants' base claim 1,

Applicants respectfully request that the rejection of dependent claims 2-8, 10, 18-20 and 24 be withdrawn for the same reasons discussed.

Lastly, claim 28 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al., U.S. Patent No. 5,627,557 in view of Yamazaki et al., U.S. Patent No. 6,335,716 and Parks, U.S. Patent No. 5,471,225 for reasons stated on pages 11-12 of the Office Action (Paper No. 3). Specifically, in support of this rejection, the Examiner further cites Parks '225 for allegedly disclosing the "image signal generating means having a reference voltage generating circuit using a poly-Si thin film resistor". However, this citation is also misplaced. Accordingly, Applicants respectfully traverse the rejection for reasons discussed herein below.

Base claim 28 defines an image display apparatus comprising:

> a plurality of display pixels arranged in a matrix in order to provide image display, each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;
> image signal generating means for outputting an image signal based on digital display data;
> a group of signal lines for connecting said image signal generating means to a group of pixel switches; and
> display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches, at least said plurality of display pixels, said group of signal lines and said image signal generating means being formed on a single transparent substrate,
> wherein said image signal generating means has a reference voltage generating circuit using a boron-doped polycrystalline Si (poly-Si) thin-film resistor.

As expressly defined in Applicants' base claim 28, the "image signal generating means has a reference voltage generating circuit using the boron-doped polycrystalline Si (Poly-Si) thin film resistor." Such a feature is described as follows.

> "However, since boron (B) does not occur such segregation, the resistance values are stable, and in addition the sheet resistance value

is an appropriate valve of several k." See page 12, lines 11-13 of Applicants' specification.

"Therefore, the poly-Si thin film doped with boron (B) is not suitable for the gray scale voltage generating resistor 53 because the electric power consumption is small, and the area is not large, and the values of generated gray scale power source voltage are stable." See page 12, lines 11-15 of Applicants' specification.

"Table 2 shows measured values of dispersion in sheet resistance of a boron (B) doped poly-Si thin film and a phosphorus (P) thin film.

Since the dispersion in sheet resistance of the phosphorus (P) thin film is above 4 times as large as that of the boron (B) doped poly-Si thin film." See page 12, lines 15-18 of Applicants' specification.

No where in Yamaguchi '557, Yamazaki '716 or Parks '225 is there any disclosure of Applicants' claimed "reference voltage generating circuit using the boron-doped polycrystalline Si (poly-Si) thin film resistor" as defined in Applicants' base claim 28. Since Yamaguchi '557, Yamazaki '716 or Parks '225 fail to disclose and suggest key features of Applicants' base claim 28, Applicants respectfully request that the rejection of Applicants' base claim 28 be withdrawn.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 503.40029X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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EXHIBIT A:

Marked-up Specification

TITLE OF THE INVENTION

IMAGE DISPLAY APPARATUS AND DRIVING METHOD THEREFOR

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal image display apparatus, and more particularly, the invention relates to a liquid crystal image display apparatus which can display an image with low power consumption.

A conventional image display apparatus technology will be described below, with reference referring to FIG. 19, which

FIG. 19 is a diagram showing the construction of a TFT liquid crystal panel using a conventional technology. Pixels 100 each having a liquid crystal capacitor 101 and a pixel switch 102 are arranged in the form of a matrix, and a gate of the pixel switch 102 is connected to a gate line shift register 104 through a gate line 103. Further, a drain of the pixel switch 102 is connected to a DA converter 106 through a signal line 105. On the other hand, each of memory cells of a frame memory arranged in the form of a matrix is composed of a memory capacitor 111 and a memory switch 112, and a gate of the memory switch is connected to a word line shift register 114 through a word line 113, and a word line selection switch 115 arranged at the end of the word line. On the other hand, one end of each of the memory switches is connected to a data line 116. A data input circuit 117 is arranged at one end of the data line 116, and a sense amplifier 108 and a latch circuit 107 are arranged at the

other end of the data line 116. An output of the latch circuit 107 is connected to the DA converter 106. The above-described constituent elements are formed using poly-Si TFT on a single substrate.

The operation of the TFT liquid crystal panel conventional example will be described below. At the time of writing, image data from the data input circuit 117 is written in the memory cells on a row selected by the word line shift register 114 and the word line selection switch 115, similar to a general DRAM (dynamic random access memory). Similarly, the image data of the memory cells on the row selected by the word line shift register 114 and the word line selection switch 115 is input to the sense amplifier 108 through the data line 116 so as to be latched by the latch circuit 107. The latched image data is converted to an analogue signal by the DA converter 106 and is output to the signal line 105. At that time, the gate line shift register 104 is scanned in synchronism with the word line shift register 114, and the gate line shift register 104 sets the pixel switch 102 on a given row to the ON-state through the gate line 103. Thereby, the analogue signal is written in the liquid crystal capacitor 101 of the given pixel 100, and accordingly, the image can be displayed using the liquid crystal based on the read-out image data.

The above-described apparatus conventional technology is described in detail, for example, in Japanese Patent Application Laid-Open No.11-85065(1999).

According to the conventional technology described above, by driving the word line 113 of the frame memory and the gate line 103 of the pixel portion with an equal driving frequency, it is possible to avoid an interference noise caused by leaking of a word line clock signal of the frame memory into the displayed image.

However, in the above-mentioned conventional technology, low power consumption of the image display apparatus is not sufficiently taken into consideration. This problem will be described below.

From the viewpoint of improving the yield by reducing the area and number of pixels, the frame memory is not formed by a SRAM (static random access memory), but is typically formed by a DRAM, as described above. However, when a general DRAM cell structure, which is typically composed of one transistor and one capacitor, which has been common, is used, a circuit having a large penetration current can not help being employed as the sense amplifier 108, because it is necessary to amplify a very small signal below several tens mV. This is a big problem from the viewpoint of low power consumption of the device.

Further, from the viewpoint of driving the DRAM cell, differently from the conventional example in which writing, refreshing and reading are separately considered, power consumption must be further reduced by organically combining writing, refreshing and reading or by modifying the driving method.

SUMMARY OF THE INVENTION

According to an embodiment in accordance with the present invention, an image display apparatus comprises a plurality of display pixels arranged in a matrix in order to perform image display, the display pixel having a pixel electrode and a pixel switch connected to the pixel electrode in series; a plurality of memory elements for storing display data; an image signal generating means for outputting a given image signal based on the display data; a group of signal lines for connecting the image signal generating means to the group of pixel switches; and a display image selection means for writing the image signal in a given display pixel through the group of signal lines and the group of pixel switches, wherein each basic unit of the memory element comprises a memory switch; a memory capacitor connected to the memory switch; an amplifier FET of which a gate is connected to the memory capacitor; and a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor.

After coming of the 4kbit-DRAM products into the market, employment of (one transistor + one capacitor) cells has become general in the field of DRAM in order to make the dimension of the memory cell as small as possible. On the other hand, the idea of the above-mentioned construction of memory cell is effective for an image display apparatus which needs to make power saving and

small area compatible.

According to an embodiment in accordance with the present invention, a method of driving an image display apparatus is that the image display apparatus comprises a plurality of display pixels arranged in a matrix in order to perform image display, the display pixel having a pixel electrode and a pixel switch connected to the pixel electrode in series; an image signal generating means for outputting a given image signal based on display data, the image signal generating means having a plurality of memory elements for storing the display data; a group of signal lines for connecting the image signal generating means to the group of pixel switches; and a display image selection means for writing the image signal in a given display pixel through the group of signal lines and the group of pixel switches, wherein each basic unit of the memory element comprises a memory switch; a memory capacitor connected to the memory switch; and a refreshing operation means for performing a preset refreshing operation to a signal charge stored in the memory capacitor, and operation of reading the display data from the memory element is included in the refreshing operation to the memory element using the refreshing operation means.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a diagram showing the construction of a first embodiment of a liquid crystal display panel.

FIG. 2 is a circuit diagram showing the circuit of a basic unit of a memory cell in the first embodiment.

FIG. 3 is a circuit diagram showing the construction of a single unit of a latch circuit in the first embodiment.

FIG. 4 is a circuit diagram showing the circuit of a clocked inverter in the first embodiment.

FIG. 5 is a circuit diagram showing the construction of a single unit of a DA converter in the first embodiment.

FIG. 6 is a diagram showing the layout of a pixel in the first embodiment.

FIG. 7 is a diagram showing the layout of a memory cell in the first embodiment.

FIG. 8 is a timing chart showing the operation timings in the first embodiment.

FIG. 9 is a schematic diagram showing the construction of a second embodiment of a liquid crystal display panel.

FIG. 10 is a circuit diagram showing the circuit of a basic unit of a memory cell in a third embodiment.

FIG. 11 is a schematic diagram showing the construction of a fourth embodiment of a liquid crystal display panel.

FIG. 12 is a schematic diagram showing the construction of a fifth embodiment of a liquid crystal display panel.

FIG. 13 is a circuit diagram showing the construction of a single unit of a latch circuit in the fifth embodiment.

FIG. 14 is a schematic diagram showing the construction of a sixth embodiment of a liquid crystal display panel.

FIG. 15 is a circuit diagram showing the circuit of a basic

unit of a memory cell in the sixth embodiment.

FIG. 16 is a diagram showing the construction of a seventh embodiment of a liquid crystal display panel.

FIG. 17 is a diagram showing the construction of a single unit of a latch circuit in the seventh embodiment.

FIG. 18 is a diagram showing the construction of an eighth embodiment of an image browser.

FIG. 19 is a diagram showing the construction of a TFT liquid crystal panel using a conventional technology.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(Embodiment 1)

A first embodiment in accordance with the present invention will be described below, referring to FIG. 1 to FIG. 8 and Table 1 and table 2.

Initially, the construction of the present embodiment will be described.

FIG. 1 is a diagram showing the construction of the embodiment of a polycrystalline Si-TFT liquid crystal display panel.

Pixels 10 each having a liquid capacitor 1 and a pixel switch 2 are arranged in a matrix, and the gate of the pixel switch 2 is connected to a gate line register 4 through a gate line 3. The drain of the pixel switch 2 is connected to a DA converter 6 through a signal line 5. On the other hand, each of memory cells 11 of a frame memory arranged in a matrix is connected to a word line 12 and

read-out line 13, both extending in the x-axis direction, and data lines 22 and a common drain line 21, both extending in the y-axis direction. Therein, a word line buffer 14 is arranged at one end of the word line 12, and a read-out line buffer 15 is arranged at one end of the read-out line 13, and, a memory y-address decoder 18 and a memory shift register 19 are selectively connected to both buffers. The word line buffer 14 and the read-out line buffer 15 each are selectively accessed by the buffer selection switch 16, and the memory y-address decoder 18 and the memory shift register 19 are selectively accessed by the address selection switch 17. On the other hand, a data line reset circuit 23 and a data line input switch 24 are arranged at one end of the data line 22, and the other end of the data line input switch 24 is connected to a data line input line 25, and the gate of the data line input switch 24 is connected to a memory x-address decoder 26. On the other hand, a latch circuit 7 is arranged at the other end of the data line 22, and the output of the latch circuit 7 is input to the DA converter 6 through a data line 22B. Therein, the gate line shift register 4 and the memory shift register 19 are driven by a clock pulse from a common input terminal 20.

Each of the constituent elements described above is formed on a single glass substrate using poly-Si TFT, and a CMOS switch constructed using a polycrystalline Si TFT is employed for each of the switches. Here, a description on the structures necessary for forming the TFT panel, such as a

color filter, a back light structure, etc. will be omitted for the sake of simplifying the description.

FIG. 2 is a diagram showing the circuit structure of a basic unit of the memory cell 11.

A memory switch 33 of which the gate, which is connected to the word line 12, is arranged in the data line 22, and the other end of the memory switch 33 is connected to a memory capacitor 31 and the gate of a memory amplifier 32. The source of the memory amplifier 32 is connected to the other end of the memory capacitor 31 and at the same time to an output switch 34. The output switch 34 is a diode-connected n-channel poly-Si TFT, and the other end of the output switch 34 is connected to the data line 22. Further, the memory capacitor 31 is also an n-channel poly-Si TFT, and the channel side is on the source side of the memory amplifier 32. The memory cell 11 is composed of three basic units, as shown in FIG. 2, but this is because the image data handled here is 3 bits.

The construction of the latch circuit 7 will be described with reference to FIG. 3, FIG. 4 and Table 1.

FIG. 3 is a diagram showing the construction of a single unit of the latch circuit which is arranged in the end portion of the data line 22. The data line 22 is connected to a CMOS inverter 36, and the output of the CMOS inverter 36 is connected to a clocked inverter 37 driven by a signal pulse $\phi 1$ and to a clocked inverter 38 driven by a signal pulse $\phi 2$. Further, the output of the clocked inverter 37 is

fed back to the data line 22, and the clocked inverter 38 outputs to the data line 22B.

FIG. 4 shows the circuit structure of the clocked inverter driven by the signal pulse $\phi 1$ as described above. Since the clocked inverter is driven by p-channel poly-Si TFTs 42, 43 and n-channel poly-Si TFTs 44, 45 and a complimentary signal pulse, the clocked inverter has three kinds of outputs of state, CMOS inverter and output disconnection.

Table 1 shows values of channel width W and channel length L of the CMOS inverter 36 in the single unit of the latch circuit shown in FIG. 2. Therein, by making the values of W/L of the p-channel poly-Si TFTs and the n-channel poly-Si TFTs composing the CMOS inverter 36 extremely unbalanced, the value of input threshold necessary for inverting the output of the CMOS inverter 36 can be set to a very small value. More specifically, in the concrete, the CMOS inverter 36 is driven by 5 V/0 V, but the input threshold is designed so as to be driven by 1 V, not 2.5 V.

Table 1

	W/L
pMOS	4/20
nMOS	20/4

The construction of the DA converter 6 will be described below with reference to FIG. 5.

FIG. 5 is a diagram showing the construction of a single unit (a repetitive unit) of the DA converter 6 which

corresponds to 6 lines of the data line 22B. In the present embodiment, since 3-bit image data is expressed by one set of 3 lines of the data line 22B, the DA converter for two sets of image data is included in the one single unit of DA converter. Each of the data lines 22B is selectively connected to a positive voltage selection circuit 47 or a negative voltage selection circuit 48 through an inverse input switch 46, and the outputs of the positive voltage selection circuit 47 and the negative voltage selection circuit 48 are connected to the signal line 5 through an inverse output switch 52. Therein, analogue gray scale voltages generated in a gray scale voltage generating resistor 53 are input to the positive voltage selection circuit 47 and the negative voltage selection circuit 48 through gray scale power source lines 49[7]; and, accordingly, the positive voltage selection circuit 47 and the negative voltage selection circuit 48 have the function to output analogue voltage values corresponding to the 3-bit image data. The gray scale voltage generating resistor 53 is formed particularly using a low-resistance poly-Si thin film doped with boron (B). This is a structure similar to the source and the drain thin films of the p-channel poly-Si TFT used in the present embodiment. If the gate wire or a general metallic wire is used for the gray scale voltage generating resistor 53, the electric power consumption and the area of the gray scale voltage generating resistor 53 are substantially increased because the resistance of the

gate wire and the general metallic wire is too small. On the other hand, since phosphorus (P) is apt to segregate in grain boundaries of poly-Si during a thermal process, such as any activation process, the resistance is apt to be changed due to variation of the crystals, and, accordingly, misalignment of color is apt to occur due to deviation of the values of gray scale power source voltage from the design values. However, since boron (B) does not allow to occur such segregation, the resistance values are stable, and, in addition, the sheet resistance value is an appropriate value of several kΩ/□. Therefore, the poly-Si thin film doped with boron (B) is most suitable for the gray scale voltage generating resistor 53, because the electric power consumption is small, and the area is not large, and the values of generated gray scale power source voltage are stable. Table 2 shows measured values of dispersion in sheet resistance of a boron (B) doped poly-Si thin film and a phosphorus (P) thin film. Since the dispersion in sheet resistance of the phosphorus (P) thin film is above 4 times as large as that of the boron (B) doped poly-Si thin film, it is preferable that the boron (B) doped poly-Si thin film is used for the gray scale voltage generating resistor 53.

Table 2

	sheet resistance: σ (%)
B doped poly-Si film	3.7
P doped poly-Si film	20.5

The construction of the pixel 10 will be described

with reference
below, referring to FIG. 6, which

FIG. 6 is a diagram showing the layout of the pixel 10, and illustrates, in which only the wires and the TFT portions are illustrated, in order to simplify the explanation. Particularly, the low-resistance wire using Al is illustrated by a bold line, and the contact hole is illustrated by a square. The signal line 5 is connected to the drain of the n-channel poly-Si TFT composing the pixel switch 2 with a contact hole, and the gate of the pixel switch 2 is formed together with the gate line 3 in a one-piece structure. The source of the pixel switch 2 is connected to an ITO (not shown) through a pixel electrode 56. The pixel electrode 56 is made of Al having a high reflectivity, and the present polycrystalline Si-TFT liquid crystal display panel can be used as a transmission type panel when the back light is turned on, and it also can be used as a reflection type panel when the back light is not turned on. Particularly, the display in the reflection type is characterized by low electric power consumption, and there is no needless need to say that such low electric power consumption is the main object of the present invention and is a very important consideration problem.

The construction of the memory cell 11 will be described below, while comparing it to the construction of the pixel 10.

FIG. 7 is a diagram showing the layout of the memory cell 11, and it illustrates only one basic unit of the memory cell for the sake of simplification. The low-resistance

wire using Al is illustrated by a bold line, and the contact hole is illustrated by a square, similarly to FIG. 6. The data line 22 is connected to one end of a memory switch 33 forming the gate by the word line 12. The other end of the memory switch 33 is connected to the gate of a memory amplifier 32 through an Al wire, and at the same time the Al wire forms a memory capacitor 31. The source of the memory amplifier 32 is connected to the data line 22 through an output switch 34 of a diode-connected n-channel poly-Si TFT. Further, the drain of the memory amplifier 32 is connected to the common drain line 21 through a read-out switch 61 controlled by a read-out line 13 at one end of the memory cell 11. In order to prevent a large current from transiently flowing in the common drain line 21, as to be described later, the common drain line 21 is not arranged in parallel to the word line 12, but is arranged in parallel to the data line 22.

The operation of the present embodiment will be described below, with reference to FIG. 8, which

FIG. 8 is a chart showing operation timings of various portions in the present invention, in Fig. 8, and the time axis from the left on the hand side expresses the operations of "writing to the memory", "reading out from the memory", "writing to the memory" and "pause". Further, items not particularly mentioned correspond to a waveform having an amplitude of 5V.

Initially, the operation of "writing to the memory"

will be described. The R/W selection pulse switches the address selection switch 17 to the memory y-address decoder 18, and the memory y-address decoder 18 is connected to the read-out line buffer 15 through the buffer selection switch 16 to turn on the read switch 61 on the selected address row. The reset pulse turns on the data line reset circuit 23 to reset the data line 22 to 0 V. Next, the voltage on the common drain line 21 rises up to apply the high level voltage (for example, 5V) to the drain of the memory amplifier 32 of the memory cell on the above-mentioned address row. However, if the memory capacitor 31 has been written at the high level voltage at that time, the memory amplifier 32 is turned on to propagate the high level voltage to the data line 22. Therein, the memory capacitor also serves as a bootstrap capacitor having a function to boost the gate voltage of the memory amplifier 32. On the other hand, if the memory capacitor 31 has been written at the low level voltage (for example, 0 V), the memory amplifier 32 is kept in the OFF-state, and accordingly the high level voltage of the common drain line 21 is not output to the data line 22. Therein, if the voltage of the common drain line 21 is returned to the low level voltage after that, the voltage written in the data line is held as it is. Next, when the signal latch pulse $\phi 1$ is input, the latch circuit shown in FIG. 3 provided for each of the data lines 22 is put into operation to determine the voltage of the data line to the high level voltage or the low level voltage by operation of the clocked inverter 37.

Therein, the reason why the threshold of the inverter 36 is lowered is to cover the voltage output from the memory amplifier 32 to the data line 22 when the voltage is insufficient. Therein, similarly to the signal latch pulse $\phi 1$, the buffer selection switch 16 is switched to the word line buffer 14 to make the word line 12 on the given row in the high level voltage. Thereby, the image data written in the data line 22 is rewritten in the same memory capacitor 31. After that, when a data input pulse is input, the memory x-address decoder 26 turns on the data line input switch of the selected address, and, as the result, the data on the data line 22 on the selected row is rewritten to a new written data which is input through the data input line 25. By the above-mentioned operation, the data of the memory cell of which the address (x, y) is selected is rewritten to the new data, and the data of the other memory cells on the same y-address is not changed.

Next, the operation of "reading out from the memory" will be described below. The R/W selection pulse switches the address selection switch 17 to the memory shift register 19, and the memory memory shift register 19 is connected to the read-out line buffer 15 through the buffer selection switch 16 to turn on the read switch 61 on the selected address row. Then, the reset pulse turns on the data line reset circuit 23 to reset the data line 22 to 0 V, and the common drain line 21 rises up to output the data of the memory cell to the data line 22, and the voltage of the

data line is determined to be the high level voltage or the low level voltage by the signal latch pulse $\phi 1$, which is the same processes as described in the operation of "writing to the memory" above. Therein, when the buffer selection switch 16 is switched to the word line buffer 14 to make the word line 12 on the given row in the high level voltage, the image data written in the data line 22 is rewritten in the same memory capacitor 31. This corresponds to the refresh operation to the memory cell, as to be described later. When the output latch pulse $\phi 2$ is output, the image data is output to the data line 22B through the clocked inverter 38. By the above-mentioned operation, the data of the memory cells on the row selected by the memory shift register 19 is refreshed, and, at the same time, output to the data line 22B. In the operation of "reading out from the memory", the operation of the gate line shift register 4 sequentially selecting the gate lines 3 is identical with the operation of the memory shift register 19 sequentially selecting the read-out lines 13 and the word lines 12. Therefore, the image data output to the data line 22B is written in the liquid crystal capacitor 1 through the DA converter 106 and the pixel switch 2 on the selected row during the horizontal scanning period after that. Further, the selection of a row of the memory cells by the memory shift register 19 is performed periodically every 1/60 second of 1 field period. Therefore, the operation of "reading out from the memory" of the memory cell can be

used as the refresh operation.

The operation of the DA converter 6, of which the construction has been described in FIG. 5, will be described below in detail. The inverse input switch 46 and the inverse output switch 52 are switched paring with each other every field period, and the circuit used for the same row of the memory cell or the same row of the pixel is alternatively exchanged between the positive voltage selection circuit 47 and the negative voltage selection circuit 48. This is because it is necessary to switch the positive and negative voltage output to the signal line 5 in order to perform alternating current drive of the liquid crystal capacitor. However, the area occupied by the DA converter can be made smaller by alternatively using the voltage selection circuits 47, 48.

Finally, the operation of "pause" will be described. In a case where it is not in the timing of reading to the memory cell and any written data is not transmitted, all the clocks are stopped, as shown in FIG. 8. At that time, the consumption of electric power around the memory during this period can be made essentially zero, because there is no circuit under operation.

In the operations described above, during the writing of the high level voltage to the memory capacitor 31 through the memory switch 33 or during the applying of the high level voltage to the drain of the memory amplifier 32 through the read-out switch 61, the high level voltage can

be written or applied only up to the memory switch 33 or the position ((gate electrode applied voltage) - (the threshold voltage Vth of the TFT)) of the read-out switch 61. Therefore, in the present embodiment, the phenomenon is avoided by setting the driving voltage of the word line 12 and the read-out line 13 higher than that for the other circuits. More specifically, in the concrete, the driving voltage of the word line 12 and the read-out line 13 is set to 10 V, while the other pulses are 5-Volt driven. Even if such a high driving voltage is used, an increase in the electric power consumption to the total electric power is very small because the capacity of the word lines 12 and the read-out lines 13 is not so large.

In the case where the DRAM structure is employed for the memory cell, as described above, there arises a problem of leakage current from the memory capacitor 31 to the memory switch 33 due to light irradiation. Particularly, in the case where the operation of refreshing is in synchronism with the operation of writing to the pixel, as in the present invention, the required capacity of the memory capacitor 31 sometimes becomes abnormally large. Therefore, it is preferable that a black matrix shielding film is formed on the reverse surface of the glass substrate 8, particularly, on the portion of the memory cell array. Otherwise, a similar effect can be obtained by designing the optical system of the reverse surface so that light of the back light may not reach the memory cell array. Light

shielding in the upper portion of the memory cell array can be similarly considered.

In the present embodiment, each of the circuit blocks is constructed on a glass substrate using polycrystalline Si-TFT elements. However, it is obvious that a quartz substrate or a transparent plastic substrate may be used instead of the glass substrate, and that an opaque substrate, such as an Si substrate, etc., may be used by limiting the liquid crystal display method to the reflecting type.

Further, of course, it is possible that the n-type and the p-type of the TFTs in the various kinds of circuits described above and the voltage relations may be inversely constructed, or other circuit structures may be employed without spoiling the principle of the present invention.

Although it has been assumed in the above description that the image display data is of 3 bits and the gray scale voltage lines 49 are 8 parallel wires applied with different gray scale voltages, it is obvious that the gray scale voltage lines are 2^n parallel wires applied with different gray scale voltages, when the image display data is of n-bit.

In addition, although in the present embodiment the CMOS switches are used for the various kinds of switches and the n-type TFT switches are used for the pixel TFTs, the present invention can be applied when any kinds of

switch structures, including p-type TFTs, are used for them. Further, there is no need to say that various kinds of layout configurations can be applied without departing from the scope of the present invention.

(Embodiment 2)

A second embodiment in accordance with the present invention will be described below, referring to FIG. 9.

Since the main structure and the main operation of the second embodiment of a polycrystalline Si-TFT liquid crystal display panel shown in FIG. 9 are similar to those of the first embodiment, the description is omitted here. Different points of the present embodiment from the first embodiment are that the structure of the memory cell 62 is different, and that the drive wires of the memory shift register 19 and the gate line shift register 4 are separated. Description will be made below on these points.

The present embodiment is characterized by that, in the layout of the memory cells, the 3-bit unit cells composing image data are horizontally aligned in a row, and that the memory capacitor is provided as a real capacitor, but not the TFT gate capacitor. The present embodiment can substantially shorten the memory width in the y-direction by the memory cell arrangement described above, and can be operated with strong stability against noise because the memory capacitor can obtain a sufficient capacitance value even if the voltage of writing to the memory cell is a low

level voltage. Therein, by using an ITO film used in the pixel, it is possible to further provide a memory capacitor using the grounded ITO film in order to further increase the memory capacity. By additionally providing a wire to which a DC voltage is applied, a capacitor independent of the above-mentioned capacitor can be also provided using the wire, though there is a problem in that the structure becomes complicated.

Since the drive wires of the memory shift register 19 and the gate line shift register 4 are separately provided, the writing operation to the pixel array can be performed, for example, at a speed one-half of a speed of the refreshing, while the refreshing operation of the memory cell is being performed in a necessary timing. By doing so, the present embodiment can further reduce the electric power consumption.

(Embodiment 3)

A third embodiment in accordance with the present invention will be described below with reference to FIG. 10.

Since the main structure and the main operation of the third embodiment of a polycrystalline Si-TFT liquid crystal display panel are similar to those of the first embodiment, the description thereof is omitted here. The main difference between A different point of the present embodiment and the first embodiment is the circuit structure of the basic unit of the memory cell 62. Description will be made below concerning this point.

FIG. 10 is a diagram showing the circuit structure of the basic unit of the memory cell in the third embodiment, which corresponds to FIG. 2 in the first embodiment. The different point of the present embodiment from the first embodiment is that the output switch 34 is changed to a p-n junction diode 63 formed on the poly-Si thin film from the diode-connected n-channel poly-Si TFT. The p-n junction diode 63 is formed by providing an n^- impurity zone of approximately 2 μm length between a p-type impurity zone and an n-type impurity zone. Since the present embodiment simplifies the structure of the basic unit of the memory cell by using the p-n junction diode 62, both of reducing of the memory area and improving of the production yield can be attained.

(Embodiment 4)

A fourth embodiment in accordance with the present invention will be described below, referring to FIG. 11, which is a diagram showing the construction of the fourth embodiment of the polycrystalline Si-TFT liquid crystal display panel.

Since the main structure and the main operation of the present embodiment are similar to those of the first embodiment, the description is omitted here. A different point of the present embodiment from the first embodiment is the circuit structure of the memory cell 62. Description will be made below on this point.

In the present embodiment, the common drain line 21 and the read-out switch 61 are eliminated, and, at the same time, the memory amplifier 63 is directly driven by the read-out line 13, and the output switch 64 is formed by a general n-channel poly-Si TFT and the gate is connected to the read-out line 13. According to the present embodiment, the structure of the memory cell can be simplified, and both a reduction of the memory area and an improvement in the production yield can be attained. However, in the present embodiment, the read-out current to all the data lines 22 through the memory amplifier 63 needs to be supplied from one read-out line 13 in all cases. Therefore, it is necessary to reduce the resistance of the output of the read-out line buffer 15 and to reduce the resistance of the read-out line 13.

(Embodiment 5)

A fifth embodiment in accordance with the present invention will be described with reference below, referring to FIG. 12 and FIG. 13.

FIG. 12 is a diagram showing the construction of the fifth embodiment of the polycrystalline Si-TFT liquid crystal display panel.

Since the main structure and the main operation of the present embodiment are similar to those of the first embodiment, the description thereof is omitted here. The main differences between the points of the present embodiment and the first embodiment

are that the reset voltage of the data line reset circuit 65 is not 0 V, but a high level voltage, and that one end of the memory amplifier 68 is grounded to 0 V through the common drain line 66, and that the output switch 69 is constructed by a general n-channel poly-Si TFT and the gate is connected to the read-out line 13, and that the basic structure of the latch circuit 67 is changed, as will be described later with reference to FIG. 13.

In the present embodiment, since the relation of voltage applied to the memory amplifier 68 is inverted, the output of the memory amplifier 68 is driven as the drain side. As the result, it is possible to solve the problem existing in the first embodiment that the TFT can be operated only up to the position ((gate electrode applied voltage) - (the threshold voltage Vth of the TFT)) at the time of a read-out operation. As the result, the memory cell circuit can be stably operated without setting the drive voltage of the word line 12 and the read-out line 13 higher than that of the other circuits. However, in the present embodiment, the output voltage to the data line 22 is the low level voltage when the write voltage to the memory capacitor 31 is the high level voltage, and the output voltage to the data line 22 becomes the high level voltage when the write voltage to the memory capacitor 31 is the low level voltage. That is, the write voltage level is inverted at every refresh operation, if it is left as it is. Therefore, in the present embodiment, the latch circuit 67 is modified as described below.

FIG. 13 is a diagram showing the structure of the single unit of the latch circuit, which corresponds to FIG. 3 in the first embodiment. The data line 22 is input to a clocked inverter 70 driven by inverting of the signal pulse $\phi 1$, and the output of the clocked inverter 70 is input to a CMOS inverter 71. The output of the CMOS inverter 71 is connected to clocked inverters 72, 73 driven by the signal pulse $\phi 1$ and a clocked inverter 74 driven by a signal pulse $\phi 2$. Further, the output of the clocked inverter 72 is fed back to the input of the CMOS inverter 71, and the output of the clocked inverter 73 is fed back to the data line 22, and the clocked inverter 74 is output to the data line 22B. In the present embodiment, by employing the construction described above, the voltage level of the data line 22 is inverted at the time when the latch pulse $\phi 1$ is input. By employing the latch circuit, the present embodiment can set the drive voltage of the word line 12 and the read-out line 13 to a value equal to the drive voltage for the other circuits, for example, to 5 V, while the write voltage level is prevented from being inverted for every refresh operation.

(Embodiment 6)

A sixth embodiment in accordance with the present invention will be described with reference below, referring to FIG. 14 and FIG. 15.

FIG. 14 is a diagram showing the construction of the sixth embodiment of the polycrystalline Si-TFT liquid

crystal display panel, and FIG. 15 is a diagram showing the circuit of the basic unit of the memory cell 75.

Since the main structure and the main operation of the present embodiment are similar to those of the first embodiment, the description is omitted here. Different points between the present embodiment and the first embodiment are that one end of the memory amplifier 77 is grounded to a DC high level voltage through the common drain line 76, and that the output switch 78 is constructed by the general poly-Si TFT, and the gate is connected to the read-out line 13, and further that the gate of the n-channel poly-Si TFT composing the memory capacitor 79 is connected to the common drain line 76.

The operation of the present embodiment is different from the operation of the first embodiment in that the memory amplifier 77 is simultaneously put into operation when the output switch 78 is selected and turned on because the drain side of the memory amplifier 77 is fixed to the high level voltage. However, the operation of the present embodiment is essentially similar to the operation of the first embodiment.

The present embodiment has an advantage in that the structure of the memory cell 75 is simplified compared with that of the first embodiment, because the DC voltage is applied to the one end of the memory amplifier 77 through the common drain line 76. Further, the present embodiment has an advantage in that the capacity of the memory

capacitor becomes large so as to stabilize the operation, particularly when writing to the memory cell is at the low level, because the construction of the memory capacitor 79 is a n-channel poly-Si TFT of which the gate is connected to the common drain line 76.

(Embodiment 7)

A seventh embodiment in accordance with the present invention will be described with reference below, referring to FIG. 16 and FIG. 17.

FIG. 16 is a diagram showing the construction of the seventh embodiment of the polycrystalline Si-TFT liquid crystal display panel.

Since the main structure and the main operation of the present embodiment are similar to those of the fifth embodiment, the description thereof is omitted here. The main differences between points of the present embodiment and from the fifth embodiment are that the data line 22, to which one end of the memory switch 80 is connected, is different from the data line 22 to which the memory switch 33 is connected, and that the basic structure of the latch circuit 81 is changed, as will be described later with reference referring to FIG. 17.

The difference in operation of the present embodiment from that of the fifth embodiment is that the data line 22 for inputting the image data to the memory cell 79 is different from the data line 22 for outputting the image data from the memory cell 79. Therefore, the structure of

the latch circuit used is modified as shown in described referring to FIG. 17.

FIG. 17 is a diagram showing the construction of one unit of the latch circuit in the present embodiment, and it corresponds to FIG. 13 in the fifth embodiment. The data line 22 is input to a clocked inverter 84 driven by inversion of the signal pulse $\phi 1$, and the output of the clocked inverter 84 is input to a CMOS inverter 86. The output of the CMOS inverter 86 is connected to clocked inverters 83, 85 driven by the signal pulse $\phi 1$ and to a clocked inverter 82 driven by the signal pulse $\phi 2$. The output of the clocked inverter 85 is fed back to the input of the CMOS inverter 86, and the output of the clocked inverter 83 is fed back to another corresponding data line 22, and the clocked inverter 82 outputs to the data line 22B. In the present embodiment, by employing the structure described above, the voltage level of the data line 22 is simultaneously inverted when the latch pulse $\phi 1$ is input, and it is written in the other corresponding data line 22. As described above, by employing the latch circuit 81 described above, the present embodiment can return the image data read out to the other data line 22 to the original data line 22, and, at the same time, it can set the drive voltage of the word line 12 and the read-out line 13 to a value equal to the drive voltage for the other circuits, for example, to 5 V, while the write voltage level is prevented from being inverted every at refresh operation.

(Embodiment 8)

An eighth embodiment in accordance with the present invention will be described below, referring to FIG. 18, which is a diagram showing the construction of the eighth embodiment of an image browser.

Compressed image data is input from the outside to a wireless interface (I/F) circuit 87 as wireless data based on the bluetooth standard, and the output of the wireless I/F circuit 87 is connected to a frame memory 89 through a central processing unit (CPU) and decoder 88. Further, the output of the CPU and decoder 88 is connected to a row selection circuit 93 and a data input circuit 92 through an interface (I/F) circuit 91 provided on the polycrystalline Si liquid crystal display panel 90, and an image display area 94 is driven by the row selection circuit 93 and the data input circuit 92. Further, an electric power source 95 and a light source 96 are arranged in an image viewer 97. Therein, the polycrystalline Si liquid crystal display panel 90 has the same construction and the same operation as those of the first embodiment previously described.

The operation of the eighth embodiment will be described below. The wireless I/F circuit 87 acquires the compressed image data from the outside, and transmits the data to the CPU and decoder 88. The CPU and decoder 88 receives operation of a user to execute driving of the image viewer 97 or processing of decoding the compressed

image data depending on necessity. The decoded image data is temporally accumulated in the frame memory 89, and the image data and the timing pulse for displaying the accumulated image are output to the I/F circuit 91 according to an instruction of the CPU and decoder 88. The I/F circuit 91 displays the image on the image display area by driving the row selection circuit 93 and the data input circuit 92 using these signals. Since this operation is the same as that described in the first embodiment, detailed explanation will be omitted here. The light source 96 is a back light to the liquid crystal display, but the light source 96 does not need to be lighted when the liquid crystal display is performed in the reflecting mode. A secondary battery is included in the electric power source 95, and supplies electric power for driving the whole apparatus.

According to the eighth embodiment, a high-quality image can be displayed with low power consumption based on compressed image data.

According to the present invention, it is possible to reduce consumed electric power of the image display apparatus.

EXHIBIT C:

Annotated Sheet Showing Changes to FIG. 1

FIG. 1